Offic Action Summary	Application No.	Applicant(s)	
	09/895,306	AU ET AL.	
	Examiner	Art Unit	
	Eric Chang	2185	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/09/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-31 are pending.

Specification

2. The disclosure is objected to because of the following informalities: several minor typographic errors in specification.

Appropriate correction is required.

Double Patenting

3. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefore..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*; 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

4. Claims 1-2, 5-9, 12-13, 17-18, 22, and 29 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1, 8-12, 25, and 27 of prior U.S. Patent No. 5,994,920 to Narayana et al. This is a double patenting rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,994,920 to Narayana et al.

7. As to claim 1, Narayana discloses an apparatus receiving a first read clock, a first write clock, a first look-ahead signal, a second read clock, a second write clock, a second look-ahead signal [col. 8, lines 20-30] to produce an output signal indicating if a FIFO is half-full or not half-full [col. 8, lines 32-33].

Narayana also discloses a state machine that is configured to receive a number of inputs including a look-ahead signal, a first and second read and write clock to produce an output signal indicating if a FIFO is half-full or not half-full [col. 6, lines 45-55]. Narayana further discloses an apparatus that uses two state machines, and a latch to generate a FIFO half-full signal based on the input of a programmable look-ahead signal, and a first and second read and write clocks [col. 6, lines 58-67, and col. 7, lines 1-2]. It would be obvious to one of ordinary skill in the art that if Narayana teaches a state machine that behaves the same as one of his taught apparatus that Narayana implicitly teaches a state machine that behaves the same as another of his taught apparatus – that is, one that receives a first read clock, a first write clock, a first look-ahead signal, a second read clock, a second write clock, a second look-ahead signal to produce an output signal indicating if a FIFO is half-full or not half-full, substantially as claimed.

Narayana teaches an apparatus that uses a state machine as claimed to generate a FIFO half-full signal based on the input of a first and second read clocks, write clocks, and

programmable look-ahead signals. Since an FIFO almost-full signal is an obvious variation of the FIFO half-full signal because they both indicate the status of a fullness of the FIFO between the full and empty state, it would be obvious to one of ordinary skill in the art to adjust the look-ahead signal generator for the offset threshold. For example, in for the half-full flag, the threshold for the look-ahead signal would be half of the buffer size, and for the almost-full flag, the threshold for the look-ahead signal would be higher. However, the look-ahead signal generation apparatus is outside of the scope of the invention, and the apparatus as claimed is taught by Narayana.

8. As to claim 2, Narayana discloses an apparatus comprising:

[a] a first set state machine receiving a first read clock, a first write clock, a first look-ahead signal [col. 8, lines 20-24], and a first control signal [col. 2, lines 50-52] to produce a first set_output signal [col. 8, lines 20-24];

[b] a second set state machine receiving a second read clock, a second write clock, a second look-ahead signal [col. 8, lines 25-30], and a second control signal [col. 3, line 19] to produce a second set_output signal [col. 8, lines 25-30];

[c] a synchronizer coupled to said second set state machine, receiving said first read control signal and a reset signal to produce a synchronized output signal [FIG. 1 element 19, and col. 4, lines 1-5];

[d] a latch receiving the first set_output signal and the synchronized output signal to produce a first latch_output signal indicating the FIFO half-full and a second latch_output signal indicating the FIFO is not half-full [col. 8, lines 32-33];

[e] a first logic block receiving the second latch_output signal to produce the first control signal [FIG. 1 element 15, and col. 2, lines 53-55]; and

[e] a second logic block receiving the first latch_output signal to produce the second control signal and the reset signal to the synchronizer [FIG. 1 element 18].

Narayana teaches an apparatus that uses two state machines, a synchronizer, a latch, and two logic blocks as claimed to generate a FIFO half-full signal based on the input of a first and second read clocks, write clocks, and programmable look-ahead signals. Since an FIFO almost-full signal is an obvious variation of the FIFO half-full signal because they both indicate the status of a fullness of the FIFO between the full and empty state, it would be obvious to one of ordinary skill in the art to adjust the look-ahead signal generator for the offset threshold. For example, in for the half-full flag, the threshold for the look-ahead signal would be half of the buffer size, and for the almost-full flag, the threshold for the look-ahead signal would be higher. However, the look-ahead signal generation apparatus is outside of the scope of the invention, and the apparatus as claimed is taught by Narayana.

9. As to claim 3, Narayana discloses a synchronizer apparatus further including an SR latch receiving said second set_output signal from the second set state machine configured to receive a reset signal from the second logic block [FIG. 1 element 19, and col. 2, lines 53-55]. Narayana teaches that the synchronization method further receives an external timing signal that controls the presentation of the second set_output signal from the SR latch [FIG. 1 element 22, col. 2, lines 45-47]. However, Narayana teaches that the presentation is handled internally by the first state machine instead of using a flip-flop external to said state machine [col. 3, lines 37-39]. It

would be obvious to one of ordinary skill in the art to use a read enabled clock within the state machine instead of an external flip-flop to control the presentation of the synchronization signal because it results in the same presentation of the signal to the workings of the state machine.

10. As to claim 4, Narayana discloses the external timing signal for the synchronizer comprises a free running write clock signal [col. 2, lines 45-47].

11. As to claim 5, Narayana discloses that the FIFO comprises a synchronous FIFO [col. 8, lines 38-39].

12. As to claim 6, Narayana discloses the first write clock comprises a first write-enabled clock [col. 7, lines 25-26].

13. As to claim 7, Narayana discloses the first read clock comprises a first read enabled clock [col. 7, lines 23-24].

14. As to claim 8, Narayana discloses the second write clock comprises a second write-enabled clock [col. 7, lines 25-26]. Narayana teaches that the second read and write clocks may be the same or different from the first read and write clocks, so the second write clock may also be a write enabled clock [col. 8, lines 29-31].

15. As to claim 9, Narayana discloses the second read clock comprises a second read enabled clock [col. 7, lines 23-24]. Narayana teaches that the second read and write clocks may be the same or different from the first read and write clocks, so the second write clock may also be a write enabled clock [col. 8, lines 29-31].

16. As to claim 10, Narayana discloses a first delay block configured to provide a first predetermined delay to said first set_output signal [FIG. 1 element 18, and col. 2, lines 42-43].

17. As to claim 11, Narayana discloses a second delay block configured to provide a second predetermined delay to said second set_output signal [FIG. 1 element 15, and col. 2, lines 54-55].

18. As to claim 12, Narayana discloses a delay block including a predetermined delay configured during fabrication [col. 7, lines 27-33]. Although Narayana teaches that this delay block is used in a different part of the apparatus than as claimed, it is obvious to one of ordinary skill in the art to use such a delay block to delay said first set_output signal as claimed.

19. As to claim 13, Narayana discloses a delay block wherein the predetermined delay is programmable [col. 7, lines 27-35]. Although Narayana teaches that this delay block is used in a different part of the apparatus than as claimed, it is obvious to one of ordinary skill in the art to use such a delay block to delay said first set_output signal as claimed.

20. As to claim 14, Narayana discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58]. Thus Narayana teaches that the delay block may be responsive to an externally generated signal.

21. As to claims 15 and 16, Narayana discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58]. Thus Narayana teaches that the delay block may comprise a JTAG programmable delay block and other JTAG circuitry and instructions.

22. As to claim 17, Narayana discloses a delay block including a predetermined delay configured during fabrication [col. 7, lines 27-33]. Although Narayana teaches that this delay block is used in a different part of the apparatus than as claimed, it is obvious to one of ordinary skill in the art to use such a delay block to delay said first set_output signal as claimed.

23. As to claim 18, Narayana discloses a delay block wherein the predetermined delay is programmable [col. 7, lines 27-35]. Although Narayana teaches that this delay block is used in a different part of the apparatus than as claimed, it is obvious to one of ordinary skill in the art to use such a delay block to delay said first set_output signal as claimed.

24. As to claim 19, Narayana discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the

reference [col. 3, lines 54-58]. Thus Narayana teaches that the delay block may be responsive to an externally generated signal.

25. As to claims 20 and 21, Narayana discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58]. Thus Narayana teaches that the delay block may comprise a JTAG programmable delay block and other JTAG circuitry and instructions.

26. As to claim 22, Narayana discloses a method for determining the emptiness of a memory buffer comprising: generating an almost-full flag in response to a plurality of signals comprising a first and second read, write, and look-ahead signals [col. 8, lines 20-31]; generating a not almost-full flag in response to same [col. 3, lines 4-6]; and presenting said signals to a state machine that generates an almost-full flag [col. 8, lines 20-31].

27. As to claim 23, Narayana discloses that the generation of the almost full output flag is delayed by a time delay [col. 3, lines 51-54].

28. As to claim 24, Narayana discloses that the generation of the not almost full output flag is delayed by a time delay [col. 3, lines 51-54]. Because Narayana teaches that the not almost full output flag is generated at the same time as the almost full flag, a delay in the generation of the almost full flag also delays the not almost full flag.

29. As to claim 25 and 26, Narayana discloses a programmable time delay in the generation of the almost full output flag and the not almost full output flag [col. 3, lines 51-54].

30. As to claim 27 and 28, Narayana discloses a JTAG programmable time delay in the generation of the almost full output flag and the not almost full output flag [col. 3, lines 54-58]. Narayana teaches that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference. Thus, Narayana teaches that the delay block may comprise a JTAG programmable delay block.

31. As to claim 29, Narayana discloses an apparatus comprising: the first manipulating means [FIG. 1 element 12, col. 2, lines 50-52, and col. 8, lines 20-24]; the second manipulating means [FIG. 1 element 14, col. 3, line 19, and col. 8, lines 25-30]; the synchronizer [FIG. 1 element 19, and col. 4, lines 1-5]; the latch [col. 8, lines 32-33]; the first logic [FIG. 1 element 15, and col. 2, lines 54-55]; and the second logic [FIG. 1 element 18, and col. 2, lines 42-43] substantially as claimed.

32. As to claim 30, Narayana discloses a first delay means to increase the pulse width of the first output signal [FIG. 1 element 18, and col. 2, lines 42-43].

33. As to claim 31, Narayana discloses second delay means to increase the pulse width of the second output signal [FIG. 1 element 15, and col. 2, lines 54-55].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
May 23, 2002